Appln No. 09/768,674

Amdt date January 20, 2004

Reply to Office action of October 21, 2003

## Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

## Listing of Claims:

1. (Currently Amended) A modulation stage for signal shaping comprising:

means for preliminary noise-shaping of an input signal; and discrete-time sampling means having a predetermined sampling frequency, the discrete-time sampling means being coupled to the noise-shaping means to produce an output signal with a lower transition rate with respect to said sampling frequency by a predetermined multiple; and

<u>a sampling means output clock for clocking the discrete-time sampling means to produce an</u> the output signal with a lower transition rate being fed back to the means for preliminary noise-shaping to sum with the input signal.

- 2. (Currently Amended) A modulation stage for signal shaping of Claim 1 wherein the discrete-time sampling means includes means for suppressing sampling of the input signal for a set number of clock cycles in response to the sampling means output clock.
- 3. (Previously Presented) A modulation stage for signal shaping of Claim 2 wherein the means for suppressing sampling includes means for detecting a transition in the output signal.

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## Claims 4.-6. (Canceled)

- 7. (Currently Amended) A modulation stage for signal shaping within a digital amplifier, the modulation stage comprising:
- a noise shaping network for preliminary noise shaping of an input signal; and
- a discrete-time sampling circuit having a predetermined sampling frequency, the discrete-time sampling circuit <a href="mailto:comprising a quantizer">comprising a quantizer</a> coupled to the noise shaping network; and
- a quantizer output clock for clocking the discrete-time sampling circuit to generate an output signal with a lower transition rate with respect to the predetermined sampling frequency by a predetermined multiple, the output signal with a lower transition rate being fed back to the noise-shaping network to sum with the input signal.
- 8. (Currently Amended) The modulation stage of Claim 7, wherein the discrete-time sampling circuit includes a logic circuit for generating the output of the quantizer output clock to suppress suppressing sampling of the input signal for a set number of clock cycles of a sampling frequency clock.
- 9. (Previously Presented) The modulation stage of Claim 8, wherein the logic circuit includes a transition detector for detecting a transition in the output signal.

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10. (Previously Presented) The modulation stage of Claim 7, wherein the output signal has a multi-state output, having at least three states.